circuit via gates 270-273 (Fig. 6). The low-going transition of PGMR causes ER_D to go high, resulting in VREFGATE going low, thereby disconnecting the reference VREF from the capacitors C_1 and C_2, once the time period (*e.g.*, about 160ns) is complete. This time period provides sufficient time for pre-charging of the negative regulation divider capacitors to allow proper regulation after switch 134a (Fig. 6) opens in the illustrated implementation of circuit 130.--

IN THE CLAIMS:

Please cancel claims 1, 8, 9, 11, 16, and 17 without prejudice or disclaimer, and amend claims 2, 10, 12, 18-20, and 22 as provided below. An appendix illustrating the amended claims in "marked up" form is provided at the end of this response for the Examiner's ease of reference.

1. (Cancelled)

12. (Amended) A method of erasing a core memory cell using a negative gate voltage in a semiconductor memory device, comprising:

generating an erase signal to begin an erase operation;

generating a pre-charge signal according to the erase signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

erasing the core memory cell by applying a negative gate voltage to the core memory cell using the regulated negative pump voltage;

wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

8. (Cancelled)

9. (Cancelled)

7 ~~10~~. (Amended) The method of claim ~~2~~ 1, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors comprises connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

11. (Cancelled)

8 ~~12~~. (Amended) A method of providing a negative gate voltage during a core memory cell erase operation, comprising:

generating a pre-charge signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

providing a negative gate voltage to the core memory cell using the regulated negative pump voltage;

wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

16. (Cancelled)

17. (Cancelled)

12 ~~18.~~ (Amended) The method of claim 8 ~~12~~, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors comprises connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

13 ~~19.~~ (Amended) An apparatus for pre-charging negative pump MOS regulation capacitors during a core cell erase operation in a memory device, comprising:

a switch connected between a reference voltage and the negative pump MOS regulation capacitors; and

a pre-charge control circuit providing a pre-charge pulse signal to the switch;

wherein the switch is operative to selectively connect the reference voltage to the negative pump MOS regulation capacitors according to the pre-charge pulse signal.

14 ~~20.~~ (Amended) The apparatus of claim 13 ~~18~~, wherein the pre-charge control circuit receives an erase signal during the core cell erase operation, and generates the pre-charge pulse signal for a time period, and wherein the switch connects the reference voltage to the negative pump MOS regulation capacitors during the time period.